Application Serial No. 10/701,306   PATENT
Reply to Office Action of December 21, 2004   Docket: CU-3424

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings,

of claims in the application.

Listing of claims:

1.   (currently amended) A clock divider for a DLL (Delay Lock Loop) circuit of a

synchronous memory device for synchronization of an external input clock with an

internal input clock, wherein the synchronous memory device generates a control

signal indicative of the power down condition of the synchronous memory

device, the clock divider comprising:

M (where M is an integer that is larger than 2) number of dividers

connected in series, the serially connected dividers being consecutively

referred to as first to M-th dividers,

wherein a first clock signal is inputted to the first divider and the first

divider outputs to the second divider a clock signal having half

the first clock signal frequency, and

wherein each of the second to M-th divider receives the clock signal

outputted from the formerly connected divider and outputs to

the subsequently connected divider a clock signal having the

frequency that is half the inputted clock signal frequency; and

a power-down controller for receiving the control signal, an output signal

of the (M-1)-th divider, and an output signal of the M-th divider, and selectively

outputting the an output signals.

wherein the respective dividers divide a frequency of a clock signal inputted to

~~the respective dividers into 1/2.~~

2.   (currently amended) The clock divider as claimed in claim 1, wherein the output

signal of the power-down controller has a frequency obtained by dividing the frequency

of the **first** clock signal inputted to the first divider into $1/2^M$ or $1/2^{(M-1)}$ in accordance with

a logic level of ~~a~~ **the** control signal.

3.   (currently amended) The clock divider as claimed in claim 2, wherein ~~if~~ **when**

the logic level of the control signal is **in** a first state (high level), the output signal of the

power-down controller ~~becomes~~ **is** the output **signal** of the (M-1)-th divider, and if the

logic level of the control signal is **in** a second state (low level), the output signal of the

power-down controller becomes the output **signal** of the M-th divider.

4.   (original) The clock divider as claimed in claim 3, wherein the control signal is a

clock enable signal used in the synchronous memory device.

5.   (original) The clock divider as claimed in any one of claims 1 to 4, wherein a

pulse width of a high-level state of the output signal of the first divider is the same as a

period of the input signal of the first divider, and a pulse width of a low-level state of

output signals of the second to M-th dividers is the same as the period of the input

signal of the first divider.

6.   (currently amended) The clock divider as claimed in ~~claim 6~~ **claim 1**, wherein

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the power-down controller comprises two transmission gates, and the two transmission

gates are selectively turned on/off according to the control signal.

7.   (currently amended) **In a synchronous memory device having a DLL (Delay**

Lock Loop) having a clock divider and generating a control signal indicative of

the power down condition of the synchronous memory device, the clock divider

comprising: M number of dividers connected in series, the serially connected

dividers being consecutively referred to as first to M-th dividers, wherein a first

clock signal is inputted to the first divider and the first divider outputs to the

second divider a clock signal having half the first clock signal frequency, and

wherein each of the second to M-th divider receives the clock signal outputted

from the formerly connected divider and outputs to the subsequently connected

divider a clock signal having the frequency that is half the inputted clock signal

frequency, A a clock dividing method ~~for a DLL (Delay Lock Loop) circuit of a~~

~~synchronous memory device for synchronization of an external input clock with~~

~~an internal input clock, the method~~ comprising the steps of:

~~selectively~~ outputting an output signal of ~~a~~ **the** (M-1)-th divider **as the**

output signal of the clock divider when the control signal is in a first state;

and

outputting an output signal of an M-th divider **as the output signal of**

the clock divider when the control signal is in a second state.

~~among M dividers, connected in series, for respectively dividing a frequency of~~

~~the input clock signal into 1/2.~~

8.   (new) The clock divider as claimed in claim 1, further comprising:

a clock buffer part receiving the external input clock, wherein the external input

clock passed through the clock buffer part is the first clock signal.